

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A disk array control apparatus comprising:

a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory; and

a second element constructed and arranged so that when new tasks are input to the disk array control apparatus the second element executes the new tasks as a first priority unless a number of the ~~first priority~~ new tasks and tasks in execution as the first priority exceeds a first number, and executes one of the new tasks as a second priority when the number of the high priority new tasks and tasks in execution as the first priority exceeds the first number,

wherein the first priority is higher than the second priority, and

wherein said second element adjusts a number of activated ones of the tasks according to the calculated cache hit ratio.

2. (previously presented) The disk array control apparatus as claimed in claim 1, wherein the number of activated

ones of the tasks decreases when the calculated cache hit ratio is above a prescribed value and increases when the calculated cache hit ratio is below the prescribed value.

3. (currently amended) A disk array control apparatus comprising:

a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory; and

a second element which executes new tasks input to the disk array control apparatus as a first priority unless a number of the new tasks and tasks in execution as the first priority ~~tasks in execution~~ exceeds a first number, and executes ~~one of~~ the new tasks as a second priority when the number of the new tasks and tasks in execution as the first priority ~~tasks in execution~~ exceeds the first number,

wherein the first priority is higher than the second priority, and

wherein said second element executes only the first priority tasks when the cache hit ratio is above a prescribed value and executes both the first priority tasks and the second priority tasks when the cache hit ratio is below the prescribed value.

4. (currently amended) A disk array control apparatus comprising:

a host I/O reception unit arranged so that the host I/O reception unit receives as an input an I/O process request from a host computer, the I/O reception unit generating as an output the I/O process request;

an I/O process execution unit that executes new tasks input to the disk array control apparatus as a first priority unless a number of the new tasks and tasks in execution as the first priority ~~tasks in execution~~ exceeds a first number and executes ~~one of~~ the new tasks as a second priority when the number of the new tasks and tasks in execution as the first priority ~~tasks in execution~~ exceeds the first number, wherein the first priority is higher than the second priority;

a cache hit determination unit constructed and arranged to determine whether or not the I/O process request is causing a cache hit at a disk cache memory;

a cache hit ratio monitor unit constructed and arranged to calculate and output a cache hit ratio within some period of time by using a determination result of the cache hit determination unit; and

an execution task selection unit constructed and arranged to assign each said I/O process request to either the first or second priority tasks, the execution task selection unit assigning said I/O process request to the first priority tasks when the cache hit ratio is not less than some prescribed value

and assigning said I/O process request to the second priority tasks when the cache hit ratio is less than the prescribed value.

5. (previously presented) The disk array control apparatus as claimed in claim 4, further comprising:

a task priority change unit constructed and arranged to dynamically change the second priority task to one of the first priority tasks after starting execution of the second priority task, the task priority change unit changing the one of the first priority tasks back to the second priority task at execution termination time.

6. (currently amended) A disk array control method comprising the steps of:

calculating a cache hit ratio at a disk cache memory;

inputting new tasks;

executing the new tasks as a first priority unless a number of the new tasks and tasks in execution at the first priority ~~tasks in execution~~ exceeds a first number;

executing ~~one of~~ the new tasks as a second priority when the number of the new tasks and tasks in execution at the first priority ~~tasks in execution~~ exceeds the first number, wherein the first priority is higher than the second priority; and

adjusting a number of activated ones of the tasks according to the calculated cache hit ratio.

7. (previously presented) The disk array control method as claimed in claim 6, wherein the adjusting step comprises the steps of:

decreasing the number of activated ones of the tasks when the cache hit ratio is above a prescribed value; and

increasing the number of activated ones of the tasks when the cache hit ratio is not above the prescribed value.

8. (currently amended) A disk array control method comprising the steps of:

calculating a cache hit ratio at a disk cache memory;

inputting new tasks;

executing the new tasks as a first priority unless a number of the new tasks and tasks in execution at the first priority ~~tasks in execution~~ exceeds a first number;

executing ~~one of~~ the new tasks as a second priority when the number of the new tasks and tasks in execution at the first priority ~~tasks in execution~~ exceeds the first number, wherein the first priority is higher than the second priority;

executing the first priority tasks when the cache hit ratio is above a prescribed value; and

executing both the first priority tasks and the second priority tasks when the cache hit ratio is not above a prescribed value.

9. (currently amended) A disk array control method comprising the steps of:

inputting an I/O process request from a host computer;  
determining whether the I/O process request is causing  
a cache hit at a disk cache memory;

calculating a cache hit ratio within some period of  
time based on results of the determining step;

inputting new tasks;

executing the new tasks as a first priority unless a  
number of the new tasks and tasks in execution at the first  
priority ~~tasks in execution~~ exceeds a first number;

executing ~~one of~~ the new tasks as a second priority  
when the number of the new tasks and tasks in execution at the  
first priority ~~tasks in execution~~ exceeds the first number,  
wherein the first priority is higher than the second priority;

assigning the I/O process request to the first priority  
tasks when the cache hit ratio is not less than some prescribed  
value; and

assigning the I/O process request to the second  
priority tasks when the cache hit ratio is less than the  
prescribed value.

10. (previously presented) The disk array control  
method as claimed in claim 9, further comprising the step of:

changing the second priority task to one of the first  
priority tasks after starting execution of the second priority  
task, and changing the one of the first priority tasks back to  
the second priority task at execution termination time.

11. (currently amended) A disk array apparatus comprising:

an I/O process execution unit which, when new tasks are input to the disk array apparatus, executes the new tasks as a first priority unless ~~[[the]]~~ a number of the new tasks and tasks in execution at the first priority ~~tasks in execution~~ exceeds a first number, and executes one of the tasks as a second priority if the number of the new tasks and tasks in execution at the first priority ~~tasks in execution~~ exceeds the first number, wherein the first priority is higher than the second priority; and

a processor cache memory which holds data used by said I/O process execution unit.

12. (currently amended) The disk array apparatus as claimed in claim 11, further comprising:

a priority change unit which changes, on execution of ~~[[the]]~~ one said second priority task, the priority of said one task from the second priority to the first priority, and changes, on completion of said one task, the priority of said one task from the first priority back to the second priority.

13. (previously presented) The disk array apparatus as claimed in claim 11, further comprising:

a disk cache memory which is accessed by one of the first or second priority tasks; and

a plurality of disks which are accessed by said one of the first or second priority tasks when said disk cache memory does not have data for said one of the first or second priority tasks.

14. (currently amended) A disk array control method used in an I/O process execution unit connected to a processor cache memory which holds data used by said I/O process execution unit, said method comprising the steps of:

inputting new tasks;

executing the new tasks as a first priority unless a number of the new tasks and tasks in execution at the first priority ~~tasks in execution~~ exceeds a first number; and

executing ~~one of~~ the new tasks as a second priority if the number of the new tasks and tasks in execution at the first priority ~~tasks in execution~~ exceeds the first number, wherein the first priority is higher than the second priority.

15. (previously presented) The disk array control method as claimed in claim 14, further comprising the steps of:

changing, on execution of the second priority task, the priority of said second priority task from the second priority to the first priority; and

changing, on completion of said task, the priority of said task whose priority has been changed to the first priority back to the second priority.



16. (previously presented) The disk array control method as claimed in claim 14, further comprising:

accessing, by the first priority tasks or the second priority task, a disk cache memory; and

accessing, by the first priority tasks or the second priority task, a plurality of disks when said disk cache memory does not have data for said first or second priority tasks.